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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,147	12/18/2001	Kohji Takano	JP9-2000-0304-US1	3176

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EXAMINER
LABAZE, EDWYN

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,147	TAKANO ET AL.	
	Examin r	Art Unit	
	EDWYN LABAZE	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Receipt is acknowledged of amendments filed on 6/12/2003.

2. Claims 1-16 are presented for examination.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

4. Figures 7 and 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated in the background of the invention as stated by the applicant on page 11, lines 12+. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Murakami et al. (U.S. 5,155,852).

Re claims 1 and 9: Murakami et al. discloses digital information coding system, which evenly distributes valid input data to digital signal processors comprising of a plurality of registers 430, 431, 432 (See fig. # 21 of Murakami et al.; col.18, lines 1-35); an arithmetic unit/PAU 225, for regarding, as inputs, values entered in said multiple registers (see fig. # 4 of Murakami et al.; col.2, lines 10+); and a plurality of memories 424, 425, 426 (col.18, lines 1+), wherein reading of multiple variables from said plurality of memories to the plurality of registers is performed during the same reading cycle by way of a pipeline process performed by said arithmetic unit (col.3, lines 52-67; col.4, lines 1-62).

Re claims 2 and 10: Murakami et al. teaches a system and method, wherein the arithmetic unit is a multiplier adder (col.5, lines 62-67; col.6, lines 1+) for, based on values x.sub.1, x.sub.2, x.sub.3 and x.sub.4 having an r-bit length that are respectively input to a first register 430, a second register 431, third register 432 and fourth register 433, providing a result Q for x1 + x2.x3 +x4 having a length of 2r bits or 2r+1 bits (see fig. # 21, tables 3 and 4 of Murakami et al.; and cols.19, 20, 21).

Re claims 3 and 11: Murakami et al. discloses a system and method, wherein the multiple memories include a first memory 424 and a second memory 425 (col.18, lines 51+); and wherein, at a stage for writing an operation result, which follows the operation stage of the pipeline process, lower r bits QL of said operation result Q are recorded in the first memory (col.21, lines 1+), and upper bits QH of the operation result Q, excluding the bits QL, are recorded in the fourth register, while at a stage for reading variables from the registers, which follows said writing stage, simultaneously, a variable x1 is read from the first memory and is

stored in the first register 430, and a variable x3 is read from the second memory and is stored in the third register 432 (col.19, lines 1-67).

Re claims 4 and 12: Murakami et al. teaches a system and method, wherein the first memory 312 and the second memory 313 are two-port memories having one data writing port and one data reading port (col.5, lines 26+; col.13, lines 48+; col.14, lines 60+; col.14, lines 41+; col.16, lines 66-68; col.17, lines 1+).

Re claims 5 and 13: Murakami et al. discloses a system and method, wherein the first memory is a two-port memory 349 having one data writing port and one data reading port (col.16, lines 66+), while the second memory 312, 211 is a single-port memory having one port for the writing and reading of data (col.3, lines 52+; col.15, lines 41+).

Re claims 6 and 14: Murakami et al. teaches a system and method, wherein the arithmetic unit is a multiplier adder (col.5, lines 62-67; col.6, lines 1+) for, based on values x 1, x2, x3, x4 x5 and x6, having an r-bit length, that are respectively input to a first register 430, a second register 431, a third register 432, a fourth register 433, a fifth register 439 and a sixth register 441, and for providing the operation results Q for x1 + x2.x3 + x4.x5 + x6, which have a length of 2r bits or 2r+1 bits (See Fig. # 21, tables 3 & 4 of Murakami et al.; and cols.19, 20, 21).

Re claims 7 and 15: Murakami et al. discloses a system and method, wherein the multiple memories include a first memory 424, a second memory 425 and a third memory 426; wherein, at a stage for writing an operation result, which follows the operation stage of said pipeline process, lower r bits QL of the operation result Q are recorded in the first memory 424, and upper bits QH of the operation result Q, excluding the bits QL, are recorded in the sixth register 441 (col.20, lines 1-3); and wherein, at a stage for reading variables to the registers, which

follows the writing stage, simultaneously (col.20, lines 9+), a variable x1 is read from the first memory 424 and is stored in the first register 430, a variable x3 is read from the second memory 425 and is stored in the third register 432, and a variable/unknown x5 is read from the third memory 426 and is stored in the fifth register 439 (see fig. # 21 of Murakami et al.; col.18, lines 1-67).

Re claims 8 and 16: Murakami et al. teaches a system and method, wherein the first memory is a two-port memory 349 having one data writing port and one data reading port (col.14, lines 60+), and the second memory 312 and the third memories 313 are single-port memories having one port for the writing and the reading of data (col.15, lines 40+).

Response to Arguments

7. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Goto (U.S. 5,475,828) teaches digital processor having plurality of memories and plurality of arithmetic logic units.

Ohtani et al. (U.S. 6,157,973) discloses microcomputer having memory and processor formed on the same chip to increase the rate of information transfer.

Hayakawa et al. (U.S. 6,249,858) teaches information processing apparatus having a CPU and an auxiliary arithmetic unit for achieving high-speed operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (703) 305-5437. The examiner can normally be reached on 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (703) 305-3503. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

el
Edwyn Labaze
Patent Examiner
Art Unit 2876
September 4, 2003

DIANE I. LEE
PRIMARY EXAMINER